REMARKS/ARGUMENTS

In the Office Action mailed May 23, 2008, claims 1-8 were rejected. Additionally, claims 5-7 were objected to. In response, claims 1, 2, 5, and 7 have been amended. Additionally, claims 3, 6, and 8 have been canceled and claims 9-10 have been added. Applicant hereby requests reconsideration of the application in view of the amended claims, the added claims, and the below-provided remarks.

Claim Objections

Claims 5-7 were objected to because of informalities. In response, claim 5 has been amended to replace the term "any one of the claim 2" with the term "claim 2." Claim 7 has been amended to replace the term "any one of the claim 2 or in the apparatus according to claim 5" with the term "claim 2." Additionally, claim 6 has been canceled. Applicant respectfully submits that amended claims 5 and 7 are in acceptable form.

Claim Rejections under 35 U.S.C. 101

Claims 6-8 were rejected under 35 U.S.C. 101 because the claimed invention is allegedly directed to non-statutory subject matter. In response, claim 7 has been amended to replace the term "Computer" with the term "A computer readable medium that stores a computer." Additionally, claims 6 and 8 have been canceled. Applicant respectfully submits that amended claim 7 is directed to statutory subject matter.

Claim Rejections under 35 U.S.C. 103

Claims 1-8 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto et al. (U.S. Pat. No. 5,587,962, hereinafter "Hashimoto") in view of Hackett et al. (U.S. Pat. No. 5,585,863, hereinafter "Hackett"). However, Applicant respectfully submits that these claims are patentable over Hashimoto and Hackett for the reasons provided below.

Independent Claim 1

Claim 1 has been amended to replace the phrase "characterized in that switching means operate" with the term "the method comprising: operating." As amended, claim 1 recites

> "Method of operating a driving circuit for a display system, wherein the sequence of writing and/or reading video data into and/or from a memory is controlled by means of an address sequencer, each of the memory addresses for said video data generated in the address sequencer being composed of a picture line address part or line pointer and an address part for a pixel on said picture line, the method comprising:
>
> operating the driving circuit alternately in a first mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers from a block of line pointers in address table register means with the output of pixel counting means, and in a second mode wherein a block of line pointers from a full table of line pointers in said memory is downloaded into said address table register means." (emphasis added).

Applicant respectfully asserts that Hashimoto fails to teach "*a first mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers from a block of line pointers in address table register means with the output of pixel counting means*" as recited in amended claim 1. The Office Action states that Hashimoto teaches a random access mode, which is "the same as the first mode in the instant claim." Hashimoto teaches a random access mode for writing or reading of a memory circuit (14), see Fig. 3 and column 4 lines 8-11. In the random access mode as taught by Hashimoto, a location in a memory array is accessed by supplying an address that corresponds to the memory location, see column 4 lines 14-17. However, Hashimoto does not teach that in the random access mode data addresses are generated by combining line pointers with pixel count. Thus, Hashimoto fails to teach "*a first mode wherein the address sequencer generates addresses for the video data in the memory by combining line pointers from a block of line pointers in address table register means with the output of pixel counting means*" as recited in amended claim 1.

Applicant respectfully asserts that Hashimoto also fails to teach "*a second mode wherein a block of line pointers from a full table of line pointers in said memory is downloaded into said address table register means*" as recited in amended claim 1. The Office Action states that Hashimoto teaches a serial mode, which is "the same as the second mode." Hashimoto teaches that a memory circuit (14) operates in a serial access

mode for both write and read operations, sees Fig. 3 and column 4 lines 8-11. In the serial access mode as taught by Hashimoto, data is read out from a memory in the same order in which it is stored into the memory, see column 4 lines 11-14. However, Hashimoto does not teach that in the serial access mode line pointers are downloaded. Thus, Hashimoto fails to teach that "*a block of line pointers from a full table of line pointers in said memory is downloaded into said address table register means*" as recited in amended claim 1.

Therefore, Hashimoto and Hackett fail to teach all the limitations of amended claim 1. Accordingly, Applicant respectfully asserts that amended claim 1 is not rendered obvious over Hashimoto in view of Hackett.

Independent Claim 2

Claim 2 has been amended to include all the limitations of claim 3. As amended, claim 2 includes similar limitations to amended claim 1. Because of the similarities between claim 1 and claim 2, Applicant respectfully asserts that the remarks provided above with regard to amended claim 1 apply also to amended claim 2. Accordingly, Applicant respectfully asserts that amended claim 2 is patentable over Hashimoto in view of Hackett.

Dependent Claims 3-8

Claims 5 and 7 have been amended to be in acceptable form. Additionally, claims 3, 6, and 8 have been canceled. Claims 4, 5, and 7 depend from and incorporate all of the limitations of the independent claim 2. Applicant respectfully asserts that claims 4, 5, and 7 are allowable at least based on an allowable claim 2. Additionally, claim 4 may be allowable for further reasons, as described below.

Claim 4 recites in part that "*the memory comprises a full table of line pointers for different sequences of video data to be displayed.*" Although Hashimoto teaches that an arbitration and control circuit (30) passes an address generated by a address generator (28a) to a memory array (24) so that data may be written into memory array (24), see Fig. 2 and column 5 lines 50-52, Hashimoto does not teach that the memory array (24) includes a full table of line pointers for different sequences of video data to be displayed.

Therefore, Applicant respectfully asserts that Hashimoto in view of Hackett does not teach all the limitations of claim 4.

New Claims 9-10

Claims 9-10 have been added. Support for claim 9 is found in Applicant's specification at, for example, claim 2 and claim 4 as originally filled. Support for claim 10 is found in Applicant's specification at, for example, claim 7 as originally filled.

Independent Claim 9

Claim 9 includes all the limitations of the original claim 4. Claim 9 recites in part that "*the memory comprises a full table of line pointers for different sequences of video data to be displayed.*" Although Hashimoto teaches that an arbitration and control circuit (30) passes an address generated by a address generator (28a) to a memory array (24) so that data may be written into the memory array (24), see Fig. 2 and column 5 lines 50-52, Hashimoto does not teach that the memory array (24) includes a full table of line pointers for different sequences of video data to be displayed. Therefore, Applicant respectfully asserts that Hashimoto in view of Hackett does not teach all the limitations of claim 9.

Dependent Claim 10

Claim 10 depends from and incorporates all of the limitations of the independent claim 2. Applicant respectfully asserts that claim 10 is allowable at least based on an allowable claim 2.

CONCLUSION

Applicant respectfully requests reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited.

Respectfully submitted,

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